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Finite Element Analysis of Microchip Cooling

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Abstract:

As electronic components continue to decrease in size and increase in power, thermal management becomes more important. Devices such as heat sinks and fans can help alleviate thermal problems, but add cost and manufacturing complexity to devices. More intimate knowledge of how a component behaves can allow companies to better determine the viability of a design and reduce over building.

In this project, finite element analysis was used to model a microchip from a Lexmark[®] printer. The results determined by the model were compared to data determined by testing the chip experimentally. The model was used to study the feasibility of using FEA to determine thermal parameters. In a natural convection environment, some thermal parameters of interest include Θ_{JA} , Ψ_{JT} , and Ψ_{JB} . The model was then used to perform parametric studies to better understand the effect of physical parameters on thermal properties.

Introduction:

As electronic components continue to decrease in size and increase in power, thermal management becomes more important. The heat flux out of the die of standard chip can be more than ten times the flux from a 100W light bulb [1]*. Devices such as heat sinks and fans can help alleviate thermal problems, but add cost and complexity to devices. Accurate determination of a component's thermal properties has become more important as companies seek to save money. More intimate knowledge of how a component behaves can allow companies to better determine the viability of design and avoid over building.

Inkjet printers have become a commodity in recent years, as the technology has stabilized and printer became less distinguishable. This has lead to a large decrease in printer prices. Consumers still expect a quiet, trouble-free machine that requires as little maintenance as possible. For these reasons inkjet printers often use natural convection to cool their electronic components.

When using natural convection, some thermal parameters of interest include Θ_{JA} , Ψ_{JT} , and Ψ_{JB} . Θ_{JA} is a measure of the thermal resistance between the microchip and air in a standardized test chamber. Since these values are linked to specific test conditions, they are generally used only to qualitatively compare microchips, with smaller values indicating better heat dispersion.

Ψ_{JT} and Ψ_{JB} are thermal characterization parameters that provide relationships between die to package top and die to board temperature differences at different power levels. While these values are not thermal resistances, they provide ways to estimate die temperature in application.

In this project, finite element analysis was used to model a microchip from a Lexmark® printer. This model will be used to study the chip and lead to a better understanding of its thermal properties. The results determined by the model will be compared to data determined by testing the chip experimentally.

Modeling Procedure:

The experimental data for the chip was obtained using a JEDEC standard test procedure. The standard used is available from the JEDEC [2]. The model was built to emulate this setup to allow simple comparisons of the data. Fairburn et al [3] detail this procedure and provided the experimental values used for comparison.

The analysis software used was Electroflo, from TES International. This program allows simultaneous solution of heat transfer, radiation, electrical circuit, and full CFD problems. This software met the needs for this project, and allows for increased complexity in the future.

The chip modeled is a PLCC-44. Its external dimensions are standardized and are available from many manufacturers [4]. To correctly model the chip, the internal dimensions of the package needed to be determined. A sample chip was etched and its internal dimensions measured. The dimensions found are shown in Figure 1. This chip was found to have copper heat spreader fingers emanating from the pad.

* Where [1] denotes entries in the Bibliography

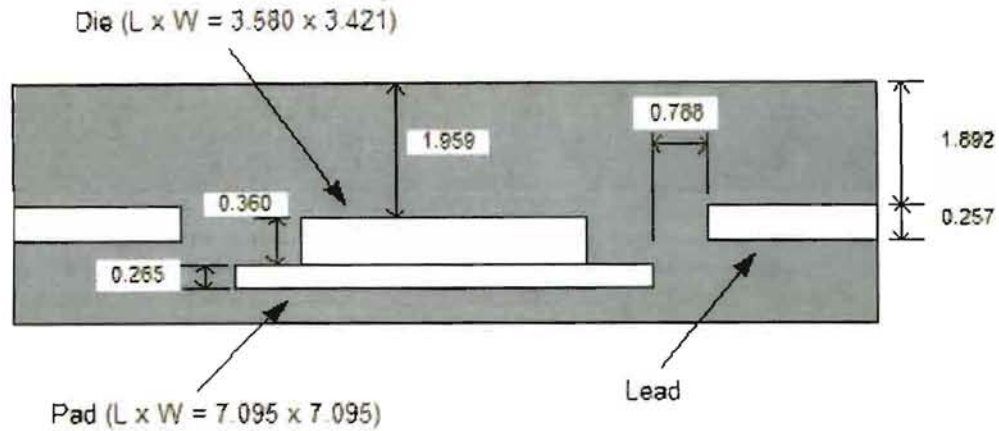


Figure 1: Internal Dimensions of Chip

The chip was modeled as an epoxy resin with a silicon die and copper pad and leads. The silicon die was the only heat-generating component in the simulation. The resistance heating of the leads and circuit board were neglected. The contact resistances at material boundaries were neglected. The copper heat spreader fingers were modeled as overlapping squares protruding from the edge of the pad. A picture of the assembly is shown in Figure 2.

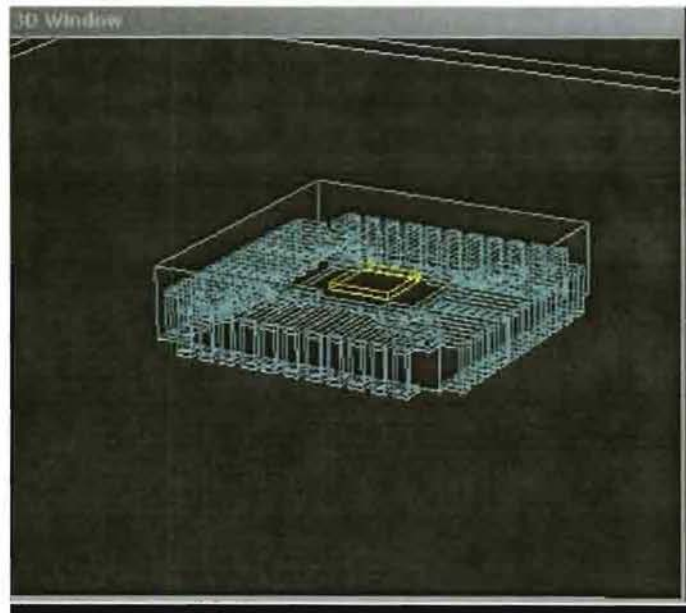


Figure 2: Model of Chip Used for Analysis

The board was initially modeled as an orthotropic material. The values for the thermal conductivity through and in-plane of the board were found by using information from Dr. Bruce Guenin, [5]. Non-standard thermal conductivities used are listed in Table

1. The default values software values for the materials of copper and silicon were used. No contact resistance was included in the model.

Table 1: Thermal Conductivities Used in Model

Material	Use	K W/mK	
		In-Plane	Across-Plane
Epoxy Resin	Case	0.63	0.63
FR4	Board Insulator	0.23	0.23
Composite	Board	20.0	0.265

The domain of this simulation was set with a length and width of 100 mm, while the top of the domain was located 20 mm above the surface of the board. The bottom of the domain was modeled to the bottom of the circuit board. The mesh used averaged 150,000 elements in the simulations, with numbers varying slightly with changes in geometry. Figure 3 shows a representative mesh used.

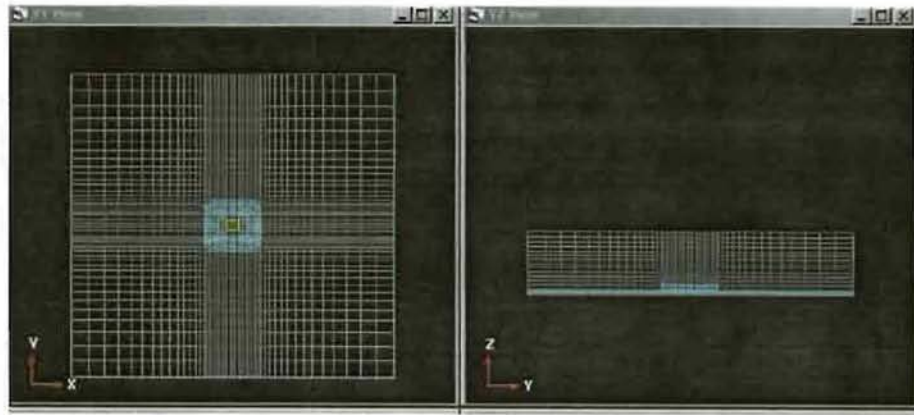


Figure 3: Representative Mesh Used for Solution

Results and Discussion:

Initial runs with this model demonstrated results that were qualitatively similar to those observed experimentally. Figure 4 shows the flow directions and temperature around the chip. The flow behaved as expected, with a maximum velocity of around 0.6 m/s. Figure 5 shows the magnitudes found for the velocity. The θ_{JA} value was the closest to the experimental results. The large percent difference between the Ψ_{JT} and Ψ_{JB} values indicates that further refining is necessary to accurately model the chip. Table 2 shows a comparison of these values for a power usage of 1 W. Complete data is presented in the appendix.

Table 2: Initial Model Results Compared to Experimental Results

	Model	Experiment	% Diff
Θ_{JA}	40.4	29.4	31%
Ψ_{JT}	2.6	5.5	71%
Ψ_{JB}	35.4	12.6	95%

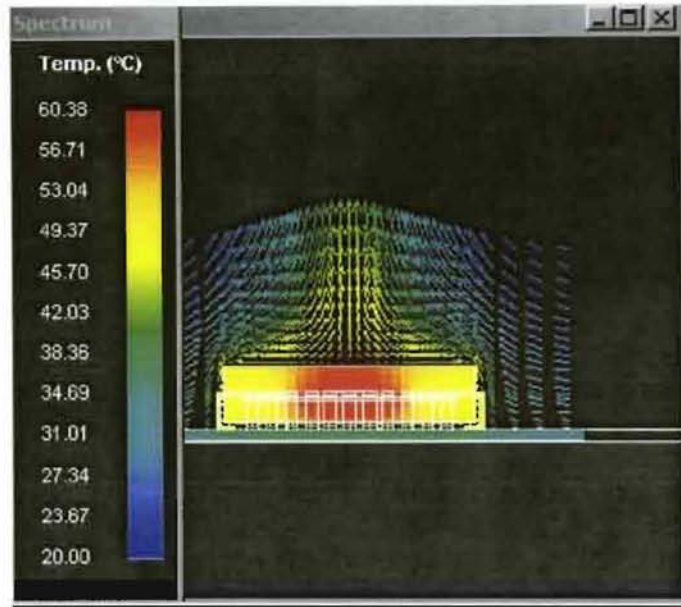


Figure 4: Flow Vectors and Temperatures Near Chip

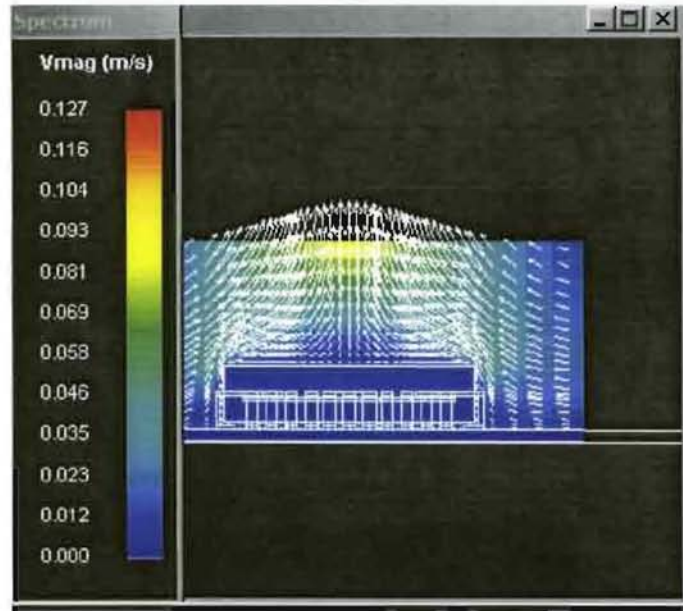


Figure 5: Air Velocity Magnitude Near Chip

The thermal conductivity of the epoxy resin was changed and the simulation rerun. The effect of changing this material property on the value of Ψ_{JT} was observed.

Figure 6 shows the results of these trials. The value of Ψ_{JT} was relatively stable with respect to thermal conductivity. For a 10% increase in K_{epoxy} , there was a 6% change in Ψ_{JT} .

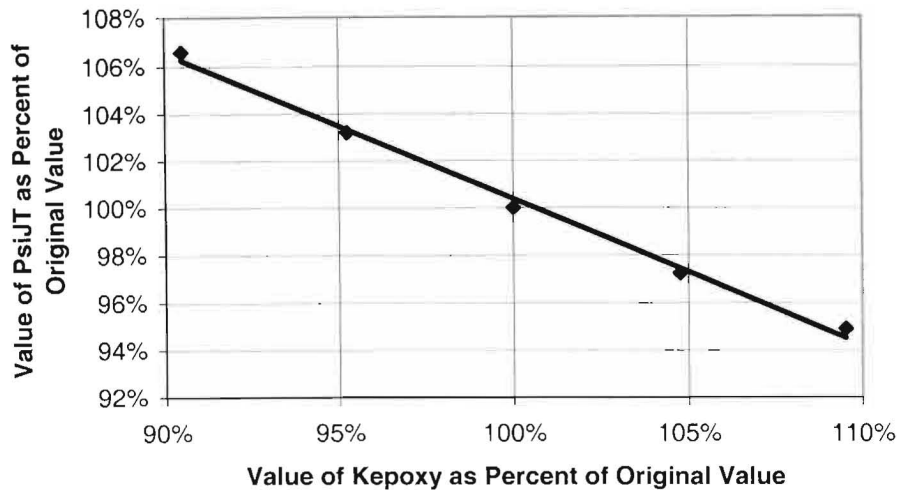


Figure 6: Effect of Thermal Conductivity on Ψ_{JT}

The widths of the 44 copper leads of the chip were changed from the standard value of 0.75 mm to 0.80 mm. This change leads to an increase in cross sectional area of 6.67%. The simulation was run again to determine the effect of this change on the cross section area. Table 3 shows the changes in the thermal numbers measured. This data shows that the effect of changing this parameter was very small. As would be expected the values of Θ_{JA} and Ψ_{JB} decreased. This is because there is less thermal resistance between the junction and the board. The value of Ψ_{JT} increased however. This indicates that this change lead to an increase in the relative temperature difference between the junction and top of the package.

Table 3: Effect of Increase of Lead Cross Sectional Area on Thermal Numbers

Lead Area Increase of 6.67%			
	Θ_{JA}	Ψ_{JT}	Ψ_{JB}
% Change	-0.75%	1.44%	-0.88%

Radiation was added to the model to determine its effects. Electroflo's thermal radiation network feature was used to set up the boundary conditions. Only surfaces with 1 mm^2 or larger area were considered. Emissivities were chosen for the materials. The epoxy resin was set at 0.95, while the board was set to 0.50. The ambient emissivity was set to 1. Table 4 shows a comparison of the thermal numbers found by the simulation when radiation was allowed and not allowed.

Table 4: Comparison of Model With and Without Radiation to Experimental Data

	No Radiation	Radiation	Experiment
Θ_{JA}	40.4	36.8	29.4
% Diff	31%	22%	
Ψ_{JT}	2.6	3.0	5.5
% Diff	71%	58%	
Ψ_{JB}	35.4	32.6	12.6
% Diff	95%	88%	

All the thermal numbers moved toward the experimental values. This shows that radiation is a significant contributor to heat transfer. This agrees with preliminary calculations that were made.

The modeling method of the board was changed to better reflect actual board construction. The test board consisted of a copper layer with a 2 oz or 0.07 mm thickness. The leads of the board were packed relatively tightly and evenly distributed. This layer was modeled as a solid sheet of 0.07mm copper. This layer was connected to a layer of FR4. The thickness of this layer was set so that the overall thickness of the board equaled the thickness used in the other simulations.

Table 5 shows a comparison of the results found using this method and the original one-layer method. The Θ_{JA} value with the new board decreased dramatically. The value determined as less than the experimentally determined value. This would be predicted by examining the model, since the real circuit board and chip would have numerous contact resistances that are not modeled. The Ψ_{JT} value diverged farther from the experimental value. Ψ_{JB} for the two-layer construction demonstrated great improvement over the one-layer construction. The one-layer construction does not properly model the heat flow into the board from the leads of the chip.

Table 5: Comparison of Board Simulation Methods

	One-Layer	Two-Layer	Experiment
Θ_{JA}	36.8	22.4	29.4
% Diff	22%	27%	
Ψ_{JT}	3.0	2.5	5.5
% Diff	58%	75%	
Ψ_{JB}	32.6	18.5	12.6
% Diff	88%	38%	

Conclusions and Recommendations:

The thermal numbers found by the model do not accurately represent their true values. The model makes a number of assumptions that could be the cause of the differences. The accuracy also varied greatly between thermal numbers.

The value of Θ_{JA} was consistently the closest of the thermal numbers to experimentally determined values. This value is the broadest of the thermal numbers and therefore the most stable through model changes. The models' Θ_{JA} values are expected

to be lower than those of the experiment. The values would be lower because no contact resistances were input to the model.

Ψ_{JT} was the thermal number that showed the least correlation with the experimental value. Even at its closest there was a percent difference between these two values of greater than 50%. This thermal number is dependent on the temperature difference across a small distance. Since the temperature difference is small, the same uncertainty in the temperatures could lead to much greater uncertainty in Ψ_{JT} and in Ψ_{JB} or Θ_{JA} .

Initially the difference in the Ψ_{JB} found by the model and experiment were very high. Further analysis showed that the changing the chip geometry did not significantly change this thermal number. When the modeling method was changed, however, the value of this parameter resembled the experiment value much more closely.

Several steps could be taken to further refine this model. Accurate numbers for the contact resistances throughout the assembly would help to move the simulation toward reality. Parametric studies of contact resistances at different locations on the chip and board could help determine which resistances are the most influential. The printed circuit board offers many options for improvement. The emissivity of the board could be changed and the copper layer in the model could be changed. Since the copper in this layer does not take up the entire area, a correction factor could be applied to the conductivity of the copper, or to the thickness of the copper.

Finite element analysis offers many tools to understand the cooling of microchips in a natural convection environment. Parametric studies help gain insight to heat transfer methods. The knowledge gained from these studies can also be used to further refine the model. With more knowledge, the Electroflo program should be able to accurately predict most thermal parameters of a chip.

Bibliography:

1. Azar, Kaveh. "The History of Power Dissipation", Electronics Cooling, 2 Jan 2000, The Cooling Zone, April 2004, <http://www.coolingzone.com/Content/Library/Papers/Jan%202000/Article%2002/Jan2000_02.html>.
2. EIA/JEDEC Standard 51-2, JEDEC Standards and Publications, Dec 1995, <<http://www.jedec.org/download/search/jesd51-2.pdf>>, April, 2004.
3. "PLCC – Plastic Leaded Chip Carrier", Practical Components, April 2004, <http://www.practicalcomponents.com/drawing_pages/plcc-drawing.htm>
4. Fairburn, Scoonover, Thomas, and Winder. "Lexmark Electronics Cooling Senior Design Project" University of Tennessee, Knoxville, May 2004.
5. Guenin, Bruce. "Conduction Heat Transfer in a Printed Circuit Board", Electronics Cooling Magazine, May 1998, The Cooling Zone, April 2004, <http://www.coolingzone.com/Guest/News/NL_APR_2001/Tutorial/ECM_Article.html>

Appendix E -

UNIVERSITY HONORS PROGRAM
SENIOR PROJECT - APPROVAL

Name: Drew Winder

College: Engineering Department: Mechanical

Faculty Mentor: Stan Johnson

PROJECT TITLE: Finite Element Analysis of Microchip
Cooling

I have reviewed this completed senior honors thesis with this student and certify that it is a project commensurate with honors level undergraduate research in this field.

Signed: [Signature] Faculty Mentor

Date: 5-30-04

General Assessment - please provide a short paragraph that highlights the most significant features of the project. Case study of natural convection cooling of electronic component from Lexmark printer. Comparison of FEA-CFD analysis to experimental data. Parametric studies of effect of model properties on thermal parameters.